Early Voltage and Saturation Voltage Improvement in Deep Sub-Micron Technologies Using Associations of Transistors

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ABSTRACT
The design of analog integrated circuits together with mixed-signal applications in deep sub-micron technologies is a difficult task, since state-of-the-art technologies and minimum channel length transistors, suitable for digital circuits, are very rarely optimized for analog block design. Non-desired effects are presenting in the shortest transistors, leading mainly to a high output conductance, which is disadvantageous for DC voltage gain stages. We present measurement results supporting the associations of transistors concept to be used in such applications: the T-Shaped Transistor (TST) [1]. The main characteristic of this association is its trapezoidal nature, with no limit on the sizes of the unit composite transistors, providing lower output conductance and saturation voltage in comparison to regular configurations. Such electrical characteristics are demonstrated by means of electrical simulations and electrical measurements of a test chip fabricated by MOSIS in an IBM 0.18µm CMOS process.

Categories and Subject Descriptors
Integrated Circuits: Types and Design Styles – Advanced technologies, VLSI (very large scale integration).
Integrated Circuits: Design Aids – electrical modeling.

General Terms: Design, MOSFET device modeling, Electrical models.

Keywords: Association of transistors, TST, TAT, Measurements, Device Modeling.

1. INTRODUCTION
The design of analog integrated circuits together with mixed-signal applications in deep sub-micron technologies is a difficult task due to the growing impact of short channel effects in the electrical characteristics of the devices. State-of-art technologies have minimum channel length transistors below 100nm and are suitable for digital circuits and not always adequate for analog blocks design. A series of non-desired effects are present, leading mainly to a high output conductance which negatively impacts gain stages. The demand for low-power systems is also causing the development of new design strategies and methodologies to deal with the relative increase of leakage currents, offset voltage and noise. Time-to-market and other economical factors require the use of fast prototyping methodologies and a high level of design automation. In this context, we present measurement results supporting the T-Shaped Transistor (TST) concept. The main characteristic of this association is its trapezoidal nature, such as TATs (Trapezoidal Associations of Transistors) [2]. The main difference here is that there is no limit on the sizes of unit transistors, which is fixed in previous TAT approach. Then, one or two more free variables are available to the designer, giving him the possibility to work with up to four dimensional parameters for the TSTs. A simplified model suitable for this type of association is presented here, considering the need to prevent or minimize second order effects which degrade circuit performance.

The main challenge is the conversion of a single rectangular transistor into an equivalent association, in such a way that negative effects related to this substitution are minimized. It is not a direct and intuitive task, because many options of associations exist. We developed a tool called LIT [3] for the analog circuits design using series-parallel associations of MOS transistors, from circuit sizing phase to layout description. Total time and costs can be reduced with this tool, moreover, design for manufacturability is also improved through layout regularity. The main characteristic of a trapezoidal association of transistors is its lower output conductance compared to a single rectangular transistor. Thus, Early voltage (VA) is also increased, leading to an advantageous configuration for analog gain stages. Another important aspect in the trapezoidal shape is the lowering of saturation voltage in comparison to cascode configurations. The goal of this work is to demonstrate such electrical characteristics by means of electrical simulations and electrical measurements of a test chip containing several test trapezoidal structures.

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SBCCI’08, September 1–4, 2008, Gramado, Brazil.
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2. TRAPEZOIDAL ASSOCIATIONS OF TRANSISTORS

The T-Shape association of transistors is characterized by the arrangement of unit MOSFET transistors in a trapezoidal format, with the drain-end side larger than the source-end side. The drain terminal, which will have the influence of more intense electric fields, is composed by a number of unit transistors in parallel or by a single transistor with sufficient width to accomplish the required drain current. The length of the transistors in the drain-side is kept always at the minimum length allowed by the target technology, because there is no need for high gain in this series device. The source-end is composed by a longer transistor or by a series association of unit transistors to achieve the desired equivalent length. There is in practice a limitation on the number of series transistors to be considered. We label the upper transistor (drain side) as MD and the remaining series association as MS. Both gates of MD and MS are connected. Considering MS to have LS larger than LD, the “T” shape is characterized.

Figure 1. Layout of an intrinsic T-Shaped Transistor

Figure 1 shows the layout of a fully customized T-Shaped transistor, with the drain terminal wider than the source terminal. This layout is neither economically viable nor technically sound, due to waste of the large area below the polysilicon gate over field oxide in the source-end. The abrupt narrowing of the channel is also a bad feature since the current flow is hindered in the MD device. Fig. 1 exemplifies, though, the shape of a trapezoidal association, which can be composed in practical layout by unit rectangular transistors connected in a series-parallel association. An association is said equivalent with respect to a rectangular transistor when some characteristics match within a certain bias region. For example, we can say that an association that has an arbitrary drain current in the saturation region for a gate-source voltage VGS=2V is equivalent to a rectangular transistor that has the same (or approximately the same) drain current for the same bias point. The relative error margin between the drain current of the association and the rectangular transistor will define the equivalence. Using the ACM (Advance Compact MOSFET) model [4], we can deduce equations that represent the T-shape association characteristics. For long channel transistors, considering two transistors in series (fig. 2a), and equating the drain currents that flow quasi-statically in MD and MS, we have:

\[
\frac{W}{L}_{eq} = \frac{ND W_{UN(MD)}}{L_{UN(MD)}+\frac{W_{UN(MD)}}{W_{UN(MS)}}L_{UN(MS)}\frac{ND}{NS}} \quad (eq. 1)
\]

where Wun and Lun are the width and length of the unit transistors, respectively, and ND is the number of unit transistors in parallel in MD and NS is the number of transistors in parallel in MS.

Figure 2. (A) TST schematic and (B) Small-signal model for a TST

3. TRAPEZOIDAL ASSOCIATIONS OF TRANSISTORS

The determination of a low frequency small-signal model is important for the calculation of electrical characteristics of a device around an operation point. In the case of a TST, we can estimate an equivalent small-signal model based on the assumption that the association is composed by two single transistors in series. We can ignore the body effect because it is not very relevant for our analysis and one can deduce more intuitive equations. Figure 2b shows the low-frequency small-signal DC model for the composite transistor [5]. With some algebraic manipulation, we can estimate the equivalent conductances and transconductances. The gate transconductance of the composite transistor \( g_{m_{TST}} \) is given by:

\[
g_{m_{TST}} = g_{ds_{MS}} \cdot g_{m_{MD}} + g_{m_{MS}} \cdot g_{m_{MD}} + g_{ds_{MS}} \cdot g_{ds_{MD}} \quad (eq. 2)
\]

According to [6], the gate transconductance of a TST is lower than that of a single rectangular transistor in strong inversion region. If we consider \( g_{m_{MD(MS)}} > g_{ds_{MD(MS)}} \), equation 2 can be approximated by:

\[
g_{m_{TST}} \approx g_{m_{MS}} \quad (eq. 3)
\]

This approximation is valid only when the MD transistor has an aspect ratio (W/L) much larger than that of the MS transistor. We can compare this effect to the source degeneration effect [7], where MS, biased in the linear region, acts like a gate voltage controlled resistor. In practice, however, the TST equivalent gate transconductance will be larger than the MS transconductance and smaller than the MD transconductance.

\[
g_{m_{MD}} > g_{m_{TST}} > g_{m_{MS}} \quad (eq. 4)
\]

This reduction in the impacts in the small-signal response, however, is compensated by the increase on the DC output resistance. The output conductance of a TST
\( g ds_{TST} = \frac{\partial I_D}{\partial V_{DS}} \) can also be estimated by the small-signal model of Figure 2:

\[
g ds_{TST} = \frac{g ds_{MD} \cdot g ds_{MS}}{g m_{MD} - g ds_{MS} - g ds_{MD}} \tag{eq. 5}
\]

The equivalent output conductance is smaller in comparison to a single rectangular transistor in all operating regions. This is one of the main advantages of TST’s, because it provides an improvement in the gain stage of an amplifier, for example, occupying a smaller area.

4. SATURATION VOLTAGE ANALYSIS

The voltage in the TST internal node \( X \) (between MD and MS in Fig. 2) is in general an unknown variable for the analog designer. It is relevant only for the calculation of drain current, transconductances and transcapacitances of the association. It can be approximated, in strong inversion, by [8]:

\[
V_X = 1 - \frac{1}{\sqrt{1 + \left(\frac{W}{L}_{MD}\right)^2 \left(\frac{W}{L}_{MS}\right)^2}} V_p \tag{eq. 6}
\]

In weak inversion by the equation:

\[
V_X \approx \phi_t \cdot \ln \left(1 + \frac{W}{L}_{MD} \cdot \frac{W}{L}_{MS}\right) \tag{eq. 7}
\]

In relation to the TST terminal voltages, it varies almost linearly with \( V_{GS} \), mainly in strong inversion, and it is constant with respect to \( V_{GS} \) when \( X \) is saturated. \( \phi_t \) is the thermal voltage. An important characteristic of the TSTs is its small saturation voltage, comparing to a cascode association. If \( \frac{W}{L}_{MD} > \frac{W}{L}_{MS} \), transistor MS operates in linear region when MD is saturated. So, the voltage between drain and source of MS is small and the equivalent saturation voltage of a composite transistor is proportional to the saturation voltage of MD. Considering \( V_{SB_{TST}} = 0 \cdot \) we have:

\[
V_X \approx V_{Dsat_{MD}} + V_{DB_{MS}} \tag{eq. 8}
\]

This property of a composite transistor makes its self-cascode structure ideal for use in low voltage applications, substituting the conventional cascode structure, which has a larger saturation voltage [9]. The equivalent saturation voltage of a TST is proportional to the pinch-off voltage, which is the same for MD and MS (proportional only to \( V_{GS} \)). As 

\[
V_{Dsat_{MS}} < V_{Dsat_{MS}} \cdot V_{Dsat_{MS}} \cdot V_{Dsat_{MS}} \cdot V_{Dsat_{MS}}
\]

In a first order analysis, we can estimate 

\[
V_{Dsat_{MS}} = V_{GS_{TST}} = V_T \cdot \text{i.e., the same of a single transistor.}
\]

Some works have demonstrated the use of self-cascodes in low-voltage low-power applications operating in weak and moderated inversion, mainly in current mirrors with high output impedance [10]. The cascode version of the current mirror is often used with the objective to provide a smaller output conductance and, consequently, a smaller difference in the copy current in relation to the reference current [11]. However, the minimum output voltage is limited to \( V_{out_{min}} = V_T + 2 \cdot V_{DS} \), being \( V_{DS} \) the amount of \( V_{GS} \) that exceeds \( V_T \). Obviously, \( V_{out_{min}} \) can be reduced with the increase of the transistors aspect ratios and gate-source voltage adjustment. However, using TSTs, we can obtain a small minimum excursion with less silicon area. It can be achieved because, for the TST version \( V_{out_{min}} = V_T + V_{DS} \). This is the same \( V_{out_{min}} \) obtained with single transistor. The advantage of TST version is that it provides a smaller output conductance.

5. CHARACTERIZATION

In order to verify the electrical behavior of T-Shaped transistors, several associations were prototyped in a test chip in IBM 0.18um CMOS process. The microphotograph of the prototyped chip is shown in Figure 3. The first association, called TAT1, is composed by 6 unit transistors of equal sizes and minimum channel length (\( W=2\mu m \) and \( L=0.18\mu m \)): 5 in parallel at the drain-end and 1 at the source-end. Figure 4a shows the schematic of the association. The second association, TAT2, is similar to TAT1, but the source-end is composed by a \( 3 \times 3 \) association, as can be seen in Figure 4b. Finally, the third association (TAT3) is a \( 5 \times 6 \) rectangular association of unit transistors (Figure 4c). Figure 5 shows the layout of the prototyped associations. The three associations have the same theoretical \( (W/L)_{eq} = 10\mu m/1.08\mu m \), according to equation 1. A single long channel test transistor (Mref) with \( W=10\mu m \) and \( L=1.08\mu m \) is fabricated on the same chip for comparison purposes.
The measurements of drain current for the three associations are shown in Figure 6. We can see that, for the same value of VGS, the drain current of TAT1 is degraded when compared to the reference single transistor. This is due to short channel effects - such as carrier velocity saturation – which are more pronounced in unit minimum-length (180nm) transistors. To its advantage, the TAT1 has, for the same bias, smaller output conductance, as can be seen in Figure 7. Another important aspect is that the output conductance is proportional to \([\frac{(W/L)_M}{(W/L)_D}]\), i.e., it is proportional to the association asymmetry.
Dividing the output conductance by drain current \((VA = gds/ID)\) we obtain the Early Voltage, which indicates the quality of the device in saturation region. Figure 8 shows the electrical measurement of VA versus VDS, demonstrating the high Early Voltage of association TAT1 in comparison to the other associations and to the equivalent single transistor. This happens due to the increase in the equivalent channel length in a trapezoidal association. For the gate transconductance, Figure 9 shows the degradation of TAT1 with respect to the single transistor Mref. Short-channel effects in the unit transistors also contribute to these results. However, the figure shows that TAT2 has good performance, caused by the correct sizing of MD, which minimizes the degradation. Another important characteristic is the \(gm/ID\) versus ID/(W/L), curves shown in Figure 10. Here, we can see that \(gm/ID\) is degraded in weak and moderated inversion for the associations, but it is similar or larger than the single transistor in strong inversion.

Figure 10. Measurement result for NMOS \(gm/ID \times ID/(W/L)\) – VDS = 1.8V

5.1 Electrical simulation of current mirrors
To visualize the effect of a low saturation voltage in the TSTs, we performed the electrical simulation of current mirrors in 4 different versions: single, TST, cascode and cascode TST. Their schematics are shown in figure 11. In figure 12 we plot the output current versus output voltage for a reference current of 50\(\mu\)A for the 4 current mirror versions. The effect of reduction of the saturation voltage in the TSTs is visible, which is an advantage of this association over the cascode configuration. Obviously, the cascode TST version is less viable, because it presents a minimum signal excursion equal to the cascode version.

6. CONCLUSION
In this paper, we presented electrical measurements and electrical simulations of trapezoidal associations of transistors in deep sub-micron technologies, demonstrating the advantages they have in comparison to a single rectangular transistor. The output conductance and Early Voltage are improved, at the expense of a lower gate transconductance. Also, saturation voltage is smaller compared to a conventional cascode configuration, what makes the trapezoidal associations very suitable for current mirrors blocks. We believe that these electrical characteristics, combined with layout regularity and design automation of layout made possible by the regular association [3], make these types of associations an important alternative for coping with the short channel effects in deep sub-micron analog design in digital CMOS technologies.
7. ACKNOWLEDGMENTS
The authors gratefully acknowledge the support of MOSIS for education chip prototyping and the CNPQ/PNM and CAPES agencies for scholarship and grant supports.

8. REFERENCES